International Journal of Multidisciplinary Research and Development

Volume :2, Issue :4, 283-285
April 2015
www.allsubjectjournal.com
e-ISSN: 2349-4182
p-ISSN: 2349-5979
Impact Factor: 3.762

Shaikh Tanjila
B.E.Electronics Univercity of Pune Pravara Rural Engg. College Loni, Tal-Rahata, Dist-Ahemednager, India

Khangel Swapnil
B.E.Electronics Univercity of Pune Pravara Rural Engg. College Loni, Tal-Rahata, Dist-Ahemednager, India

Pagare Sarla
B.E.Electronics Univercity of Pune Pravara Rural Engg. College Loni, Tal-Rahata, Dist-Ahemednager, India

Correspondence:
Shaikh Tanjila
B.E.Electronics Univercity of Pune Pravara Rural Engg. College Loni, Tal-Rahata, Dist-Ahemednager, India

Implementing an I2C Bus on FPGA

Shaikh Tanjila, Khangel Swapnil, Pagare Sarla

Abstract
The I2C protocol was given by Philips Semiconductors in order to allow faster devices to communicate with slower devices and also allow devices to communicate with each other over a serial data bus without data loss. we designed home automation using I2C bus which makes it more easier to implement it.

Keywords: I2C Bus, slave,master, Finite state machine

1. Introduction
The EEPROM, ADC and RTC will require an interface for communication between them. Due to that I2C bus is used as an interface between EPROM, ADC and RTC. It is used to minimize system-level interconnect. This simplifies the system level design and the design of the mother- board and associated chip-boards. Moreover transmitting information over the I2C bus will improve system performance since the transmission of digital data is much less susceptible to interference from environmental noise sources.

2. The I2 C bus
The I2 C (Inter IC) bus is a simple bi-directional serial bus that supports multiple masters and slaves. It consists of only two lines; a serial bi-directional data line (SDA) and a serial bi-directional clock line (SCL). Within the I2 C bus specifications, a standard mode with a maximum clock rate of 100k Hz and a fast mode with a maximum clock rate of 400k Hz are defined.
Each device connected to the I2 C bus is software addressable by a simple master/slave relationship and unique address exists at all times among the devices. The device that controls the sending and receiving of messages by controlling the bus access is referred to as the *master*.
Devices that are controlled by the master are the *saves*. Both the master and the slave can send
and receive messages. A device that sends data onto the bus is referred to as the *transmitter* and a device receiving data is referred to as the *receiver*.
More than one master and more than one slave can all co-exist on the same I2 C bus. However, the bus is always controlled by a single master who is responsible for generating the serial clock, and controlling the bus access by initiating and terminating a message transfer.

3. I2C Bus Specifications
The I2C Controller Bus is a bi-directional serial bus,bi-directional that provides a simple and efficient method of data transmission over a short distance between many devices. Basically I2C bus provides good support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It has a low-bandwidth, short- distance protocol. It is easy to use to link multiple devices together since it has a built-in address [1][2]. The two I2C signals are serial data (SDA) and serial Clock (SCL) as shown in Figure 1.The device that initiates a transaction on the I2C bus is termed the master. The master normally controls the clock signal and process. A device being addressed by the master is called a slave [1][2]

The I2C protocol supports multiple masters, but most system designs include only one but in some complex application it can contain more than one. There may be one or more slaves on the bus. Both masters and slaves can receive and transmit data bytes. Standard I2C devices operate up to 100Kbps, while fast-mode devices operate at up to 400Kbps. Most of the I2C devices available today support 400Kbps operation. Higher-speed operation may allow I2C to keep up with the rising demand for bandwidth in other applications and multimedia.

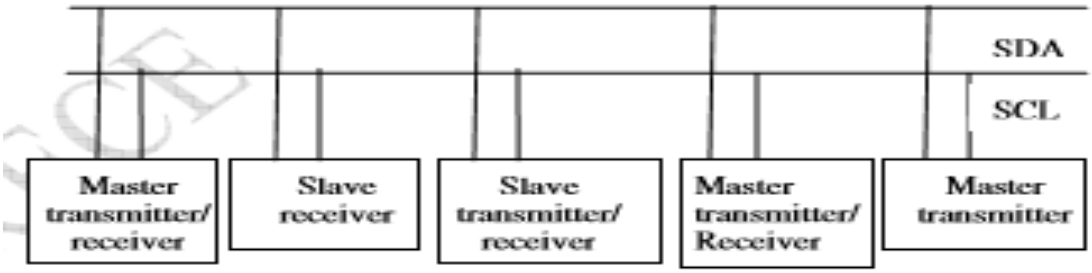

Fig. 1 I2C bus configuration using masters and slaves

4. I2C Protocol

The SDA and SCL lines are bi-directional lines connected to a positive voltage supply through a pull- up resistor. The bus is free when these lines are 'high'. The data on the SDA line is valid only when the SCL line is 'high'. Change of data is allowed when SCL line becomes 'low'. During data transfer, the master generates the START and STOP conditions, which are unique conditions and are shown in Figure[2].

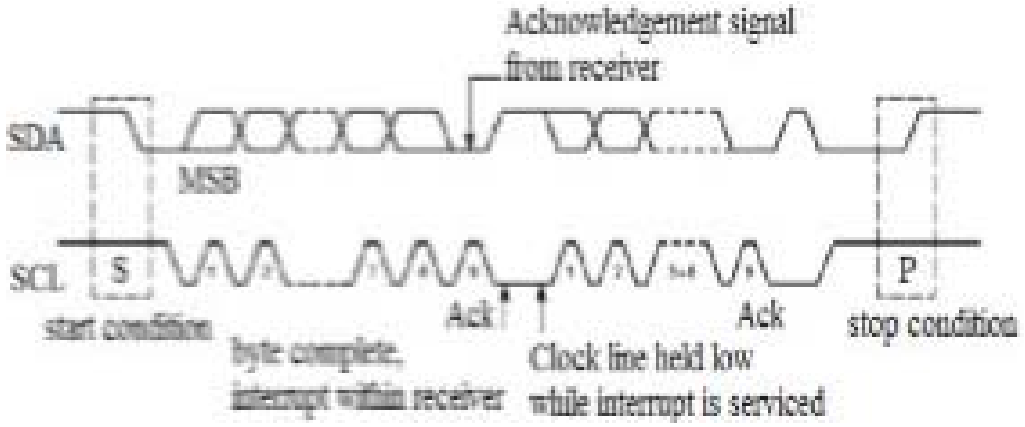

Fig 2: I2C Protocol

5. I2c Bus Controller Design

I2C protocol consists of four parts 1) START signal generation,2) Slave address transfer,3) Data transfer,4) STOP signal generation.

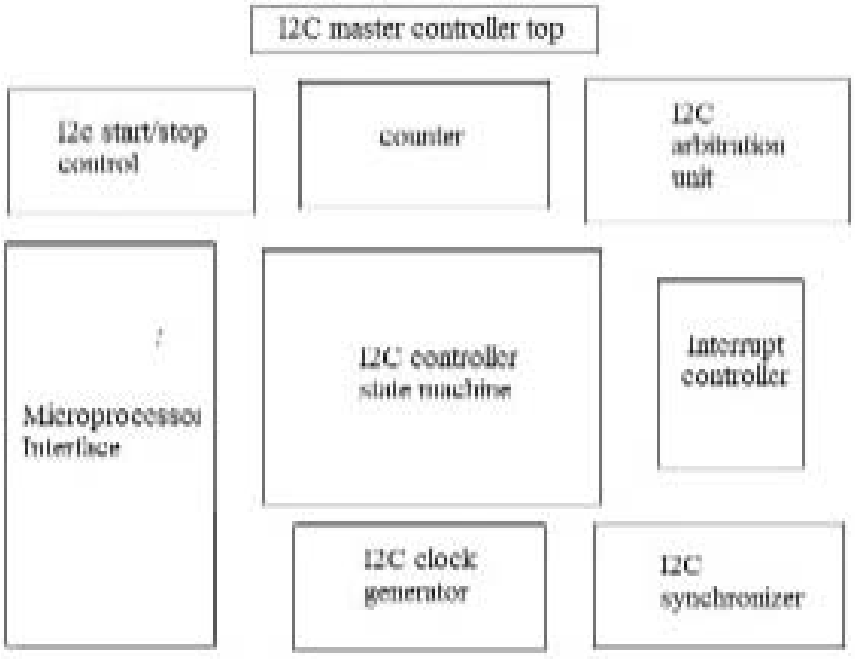

Fig 3: Basic Controller Design

6. I2c Bus Architecture

It consists of a master and a slave connected using I2C bus. The SDA line is connected to a positive supply voltage through a pull up resistor. The SCL line is not connected to a pull up resistor as there is only one master. Designing the I2C master controller

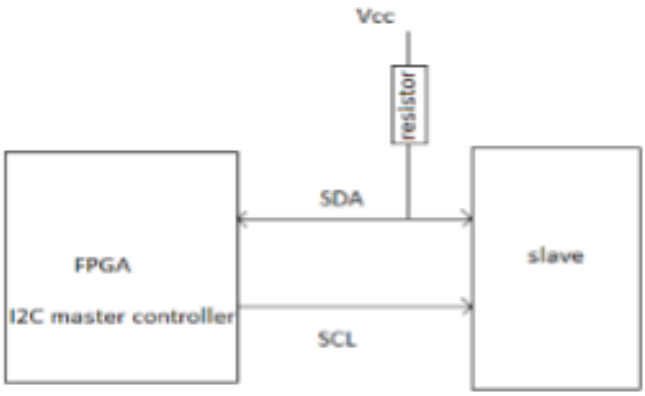

Fig 4: I2C Bus Architecture

For designing the I2C master controller is to use a finite state machine (FSM). We can easily implement finite state machine by writing VHDL

Finite State machine

A finite state machine is a sequential circuit that uses a finite number of states to keep track of its history of operations, and based on this history and its current inputs, determine what to do next.

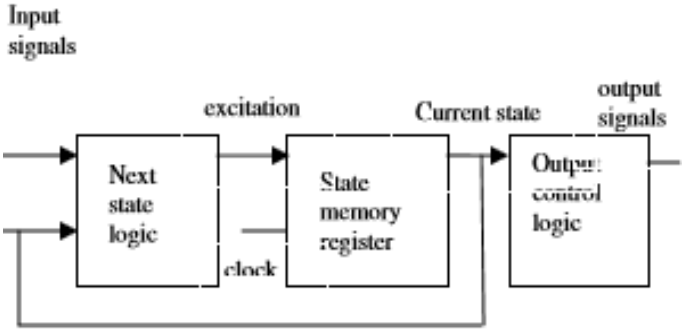

Fig 5: Block diagram of finite state machine

A sequential circuit is one where its outputs are dependent on its history of operation and its current inputs.

7. Result Analysis

Here the I2C bus is used for home automation in which the humidity and temperature can be easily termined using xilink 7.10 .The device utilization summary is given below

1. Program stimulation get so much easy
2. Interface becomes handy

8. Conclusion

The result shows that minimal resources are utilized. The design process is simplified using I2C bus.The designer can write his design description without choosing any specific fabrication technology. If a new technology emerges, designers do not need to redesign the circuit. He simply input the design program to the logic synthesis tool and creates a new gate level netlist using the new fabrication technology. The logic synthesis tool will optimize the circuit in area and timing for the new technology.

References

1. Philips I2 C specifications http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf
2. Digital Logic and Microprocessor Design with VHDL, E. Hwang, Thomson, 2006. http://faculty.lasierra.edu/~ehwang/digitaldesign
3. Altera Quartus II development software, http://university.altera.com/materials/software/unv-quartus2.html.
4. Altera DE2 development board, http://university.altera.com/materials/boards/unv-de2-board.html
5. Muhammed Ali Mazidi, Janice Gillispie Mazidi & Rolin D. Mckinlay,The 8051 Microcontroller and Embedded Systems, using Assembly and C , second Edition, Pearson Education.
6. IEEE Computer Society. IEEE Standard Verilog® Hardware Description Language, IEEE Std 1364- 2001, The Institute of Electrical and Electronics Engineers, Inc, 28 September 2001